In The Claims:

1.(currently amended) A method of determining the performance of a microprocessor having a circuit emulation mode and a normal operating mode, wherein the performance of a program having a plurality of instructions is assessed, comprising the steps of:

triggering the microprocessor into the circuit emulation mode;

setting a first upper value in an instruction counter and a second upper value in a cycle counter;

resetting ~~an~~ the instruction counter and ~~a~~ the cycle counter to zero;

triggering the microprocessor into the normal operating mode and executing the program;

~~initializing~~ initiating the counting by the instruction counter such that the instruction counter increments by one when an instruction is executed, wherein the microprocessor is triggered into the circuit emulation mode when the instruction counter reaches ~~an~~ the first upper value~~, the value inside the instruction counter and the cycle counter is read to evaluate execution performance and then the microprocessor is triggered into the circuit emulation mode again~~; while ~~initializing~~ initiating the counting by the cycle counter such that the cycle counter increments by one when a timing pulse traverses a cycle, wherein the microprocessor is triggered into the circuit emulation mode when the cycle counter reaches ~~an~~ the second upper value~~, the value inside the instruction counter and the cycle counter is read to evaluate execution performance and then the microprocessor is triggered into the circuit emulation mode again~~, and the instruction counter and the cycle counter start to count concurrently ;

triggering the microprocessor into the circuit emulation mode when the program is executed to ~~a definite~~ an assessment point;

reading out the value inside the instruction counter and the cycle counter; and

evaluating microprocessor performance.

2. (original) The method of determining microprocessor performance of claim 1, wherein the method further includes the following steps:

triggering the microprocessor into the circuit emulation mode on complete execution of the program;

reading out the value inside the instruction counter and the cycle counter; and

evaluating microprocessor performance.

3. (currently amended) The method of determining microprocessor performance of claim 2, wherein the method further includes the following steps:

setting up an assessment point into a breaking point register where performance measurement is required when the microprocessor is in the circuit emulation mode;

triggering the microprocessor into the normal operating mode and executing the program;

initiating the counting by the instruction counter such that the instruction counter increments by one when an instruction is executed, wherein the microprocessor is triggered into the circuit emulation mode when the instruction counter reaches a first upper value; while initiating the counting by the cycle counter such that the cycle counter increments by one when a timing pulse traverses a cycle, wherein the microprocessor is

triggered into the circuit emulation mode when the cycle counter reaches a second upper value, and the instruction counter and the cycle counter start to count concurrently ;

~~setting up an assessment point at an instruction where execution speed is required;~~

triggering the microprocessor into the circuit emulation mode when the assessment point is encountered during instruction execution;

reading out the value inside the instruction counter and the cycle counter; and

evaluating microprocessor performance.

4. (currently amended) The method of determining microprocessor performance of claim 3, wherein the method further includes the following steps:

setting up an assessment point ~~at the start and at the end of a series of instructions~~ into the breaking point register where ~~execution speed~~ performance measurement is required;

triggering the microprocessor into the circuit emulation mode when the ~~start~~ assessment point is encountered during instruction execution;

reading out the value inside the instruction counter and the cycle counter;

triggering the microprocessor into the circuit emulation mode;

resetting an instruction counter and a cycle counter to zero;

triggering the microprocessor into the normal operating mode and executing the program;

~~initializing~~ initiating the counting by the instruction counter such that the instruction counter increments by one when an instruction is executed; while ~~initializing~~ initiating the counting by the instruction counter such that the cycle counter increments by one when a timing pulse ~~is traversed~~ traverses a cycle, wherein and the instruction counter

and the cycle counter start to count concurrently ;

triggering the microprocessor into the circuit emulation mode when the ~~ending~~ assessment point is encountered;

reading out the value in the instruction counter and the cycle counter; and

evaluating microprocessor performance.

5. (original) The method of determining microprocessor performance of claim 4, wherein the evaluation of microprocessor performance includes:

dividing the value inside cycle counter by the value inside the instruction counter.

6. (currently amended) A device for determining the performance of a microprocessor execution, comprising:

a microprocessor capable of operating in a circuit emulation mode and a normal operating mode;

an instruction counter for counting up by one whenever an instruction is executed, and when the instruction counter counts to ~~an upper limit~~ a first upper value, the microprocessor is triggered into the circuit emulation mode, ~~the values within the instruction counter and the cycle counter are read out~~; ~~and~~ while a cycle counter for counting up by one whenever one cycle of timing pulse is traversed, and when the cycle counter counts to ~~an upper limit~~ a second upper value, wherein the instruction counter and the cycle counter start to count concurrently, and the microprocessor is triggered into the circuit emulation mode~~,~~ after the values within the instruction counter and the cycle

counter are read out, and

wherein microprocessor performance is evaluated by dividing the value inside the cycle counter by the value inside the instruction counter.

7. (currently amended) A method of determining the performance of a microprocessor having a circuit emulation mode and a normal operating mode, wherein the performance of a program having a plurality of instructions is assessed, comprising the steps of:

triggering the microprocessor into the circuit emulation mode;

setting a first upper value in an instruction counter and a second upper value in a cycle counter;

resetting ~~an~~ the instruction counter and ~~a~~ the cycle counter to zero;

triggering the microprocessor into the normal operating mode and executing the program;

~~initializing~~ initiating the counting by ~~either~~ the instruction counter such that the instruction counter increments by one when an instruction is executed, ~~or~~ and by the cycle counter such that the cycle counter increments by one when a timing pulse traverses a cycle, and then the instruction counter and the cycle counter starting to count concurrently until ~~wherein the microprocessor is triggered into the circuit emulation mode~~ when either the instruction counter reaches ~~an~~ the first upper value ~~if the instruction counter is initialized, wherein the microprocessor is triggered into the circuit emulation mode when the cycle counter reaches an upper value if the cycle counter is initialized;~~ or the cycle counter reaches the second upper value, the microprocessor is triggered into the circuit emulation mode;

reading the value inside the instruction counter and the cycle counter to evaluate execution performance and then the microprocessor is triggered into the circuit emulation mode again;

resetting the instruction counter and the cycle counter to zero, setting up an assessment point into a breaking point register, and initiating the counting by the instruction counter and the cycle counter;

triggering the microprocessor into the normal operating mode and executing the program;

triggering the microprocessor into the circuit emulation mode when the program is executed to ~~a definite point~~ the assessment point ;

reading out the value inside the instruction counter and the cycle counter; and

evaluating microprocessor performance.

8. (original) The method of determining microprocessor performance of claim 7, wherein the method further includes the following steps:

triggering the microprocessor into the circuit emulation mode on complete execution of the program;

reading out the value inside the instruction counter and the cycle counter; and

evaluating microprocessor performance.

9. (currently amended) The method of determining microprocessor performance of claim 8, wherein the method further includes the following steps:

setting up an assessment point ~~at~~ into the breaking point register where ~~execution speed~~

performance measurement is required when the microprocessor is in the circuit emulation mode;

triggering the microprocessor into the circuit emulation mode when the assessment point is encountered during instruction execution;

reading out the value inside the instruction counter and the cycle counter; and

evaluating microprocessor performance.

10. (currently amended) The method of determining microprocessor performance of claim 9, wherein the method further includes the following steps:

setting up an assessment point ~~at the start and at the end of a series of instructions~~ into the breaking point register where ~~execution speed~~ performance measurement is required;

triggering the microprocessor into the circuit emulation mode when the start assessment point is encountered during instruction execution;

reading out the value inside the instruction counter and the cycle counter;

triggering the microprocessor into the circuit emulation mode;

resetting the instruction counter and the cycle counter to zero;

triggering the microprocessor into the normal operating mode and executing the program;

~~initializing~~ initiating the counting by the instruction counter such that the instruction counter increments by one when an instruction is executed;

~~initializing~~ initiating the counting by the instruction counter such that the cycle counter increments by one when a timing pulse ~~is traversed~~ traverses a cycle, wherein the instruction counter and the cycle counter start to count concurrently ;

triggering the microprocessor into the circuit emulation mode when the ~~ending~~ assessment point is encountered;

reading out the value in the instruction counter and the cycle counter; and

evaluating microprocessor performance.

11. (original) The method of determining microprocessor performance of claim 10, wherein the evaluation of microprocessor performance includes:

dividing the value inside cycle counter by the value inside the instruction counter.